WHAT IS CLAIMED IS:

1. A buffer circuit for a liquid crystal display device comprising:

a first transistor further comprising a gate connectable to an input signal, a first electrode coupled to a first power supply, and a second electrode connectable to a second power supply;

a second transistor further comprising a gate coupled to the second electrode of the first transistor, a first electrode connectable to the first power supply, and a second electrode connectable to the second power supply;

a first capacitor being connectable to the input signal storing a voltage of the input signal when connected to the input signal, and providing a first voltage to the gate of the first transistor when disconnected from the input signal;

a second capacitor further comprising a terminal coupled to the second electrode of the first transistor and the gate of the second transistor providing a second voltage at the terminal when the first transistor is turned on; and

a third capacitor coupled to the first electrode of the second transistor providing a third voltage when the second transistor is turned on;

wherein the second voltage further comprises a first offset including a gate to source voltage of the first transistor, and the third voltage further comprises a second offset including a gate to source voltage of the second transistor.

2. The circuit of claim 1 further comprising a fourth capacitor including one terminal connectable to the second electrode of the second transistor, and another terminal connectable to the first capacitor.

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3. The circuit of claim 1, the first voltage further comprising the voltage of the input signal.

4. The circuit of claim 1, the first voltage further comprising a reference voltage.

5. The circuit of claim 1, the first voltage further comprising the voltage of the input signal and offset voltages including a gate to source voltage each of the first transistor and the second transistor.

6. The circuit of claim 1, the second voltage further comprising the first voltage and an offset voltage including a gate to source voltage of the first transistor.

7. The circuit of claim 1, the third voltage being compensated by a threshold voltage each of the first transistor and the second transistor.

8. The circuit of claim 2, the fourth capacitor providing a fourth voltage when second transistor is turned on.

9. The circuit of claim 8, the fourth voltage further comprising offset voltages including a gate to source voltage each of the first and second transistors.

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10. A buffer circuit for a liquid crystal display device comprising:

a first transistor further comprising a gate connectable to an input signal;

a second transistor further comprising a gate coupled to an electrode of the first transistor;

a first capacitor being connectable to the input signal and the gate of the first transistor storing a voltage of the input signal when connected to the input signal, and providing the voltage of the input signal to the gate of the first transistor when disconnected from the input signal;

a second capacitor coupled to the gate of the second transistor providing a voltage to the gate of the second transistor including a first offset component when the first transistor is turned on; and

a third capacitor providing a voltage including a second offset component to neutralize the first offset component when the second transistor is turned on.

11. The circuit of claim 10, the first offset component further comprising a gate to source voltage of the first transistor.

12. The circuit of claim 10, the first offset component further comprising a threshold voltage of the first transistor.

13. The circuit of claim 10, the second offset component further comprising a gate to source voltage of the second transistor.

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14. The circuit of claim 10, the second offset component further comprising a threshold voltage of the second transistor.

15. A buffer circuit for a liquid crystal display device comprising:

a first capacitor being connectable to an input signal storing a reference voltage during a first period, and storing a voltage of the input signal during a second period after the first period;

a second capacitor providing a voltage including a first offset during the first period, and providing a voltage including another first offset to neutralize the first offset during the second period;

a third capacitor providing a voltage including a second offset during the first period, and providing a voltage including another second offset to neutralize the second offset during the second period; and

a fourth capacitor storing the first and second offsets during the first period.

16. The circuit of claim 15 further comprising a first transistor and a second transistor.

17. The circuit of claim 16, the first and second offsets further comprising a gate to source voltage of the first transistor and the second transistor, respectively.

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18. The circuit of claim 16, the other first and another second offsets further comprising a gate to source voltage of the first and second transistors, respectively.

19. The circuit of claim 15, the reference voltage further comprising a zero voltage.

20. A method of compensating an offset voltage in a buffer circuit for a liquid crystal display device comprising:

providing an input signal;

charging a first capacitor with a voltage of the input signal;

providing the voltage of the input signal to a first transistor;

turning on the first transistor;

storing a voltage including a first offset voltage in a second capacitor, the first offset voltage further comprising a gate to source voltage of the first transistor;

turning on a second transistor; and

storing a voltage including a second offset voltage in a third capacitor, the second offset further comprising a gate to source voltage of the second transistor.

21. The method of claim 20 further comprising compensating the input signal with the first offset voltage and the second offset voltage.

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22. The method of claim 20 further comprising storing in the second capacitor a voltage including the voltage of the input signal and an offset voltage including a threshold voltage of the first transistor.

23. The method of claim 20 further comprising storing in the third capacitor a voltage including the voltage of the input signal and including an offset voltage further including a threshold voltage of the second transistor.

24. A method of compensating an offset voltage in a buffer circuit for a liquid crystal display device comprising:

providing a reference signal;

determining a first offset for a first transistor;

storing the first offset;

determining a second offset for a second transistor;

storing the second offset;

providing an input signal different from the reference signal;

determining another first offset for the first transistor;

storing the other first offset;

determining another second offset for the second transistor;

storing the other second offset; and

neutralizing the first and second offsets with the other first offset and the other second offset.

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25. The method of claim 24, after providing the reference signal, further comprising storing a voltage of the reference signal in a first capacitor, and turning on the first transistor with the voltage of the reference signal.

26. The method of claim 25 further comprising storing the first offset in a second capacitor, and storing the second offset in a third capacitor.

27. The method of claim 26 further comprising storing the first offset and the second offset in a fourth capacitor.

28. The method of claim 25 further comprising storing the other first offset in a second capacitor, and storing the other second offset in a third capacitor.

29. The method of claim 28 further comprising storing the other first offset and the other second offset in a fourth capacitor.

30. The method of claim 24 further comprising determining the first offset as a gate to source voltage of the first transistor.

31. The method of claim 24 further comprising determining the second offset as a gate to source voltage of the second transistor.

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32. The method of claim 24 further comprising determining the first offset as a threshold voltage of the first transistor.

33. The method of claim 24 further comprising determining the second offset as a threshold voltage of the second transistor.

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